Question Paper Code : 21303

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Fourth Semester

Computer Science and Engineering

CS 2253/CS 43/CS 1252 A/10144 CS 404/080250011 – COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulation 2008/2010)

(Also Common to PTCS 2253 – Computer Organisation and Architecture for B.E (Part-Time) Third Semester – CSE – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is meant by an addressing mode? Mention most important of them.
2. State the rule for floating point addition.
3. Write the register transfer sequence to read a word from memory.
4. What is a micro-program sequencer?
5. What is meant by hazard in pipelining? Define data and control hazards.
6. Why is branch prediction algorithm needed? Differentiate between the static and dynamic techniques.
7. An address space is specified by 24 bits and the correspoding memory space by 16 bits :

   How many words are there in the virtual memory and in the main memory?
8. What is meant by an interleaved memory?
9. Distinguish between isolated and memory-mapped I/O?
10. Mention the advantages of USB.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain different types of instructions with examples. Compare their relative merits and demerits. (8)

(ii) Explain with an example how to multiply two unsigned binary numbers. (8)

Or

(b) Explain the design of ALU in detail. (16)

12. (a) Explain the design of micro-programmed control unit in detail. (16)

Or

(b) (i) Explain the execution of a three operand instruction using multiple bus organization. (8)

(ii) Write notes on nano programming. (8)

13. (a) (i) Explain a 4-stage instruction pipeline. Also explain the issues affecting pipeline performance. (10)

(ii) Explain dynamic branch prediction technique. (6)

Or

(b) (i) Explain the relation between pipelined execution and instruction feature. (6)

(ii) Describe the techniques for handling control hazards in pipelining. (10)

14. (a) (i) Draw the block diagrams of two types of DRAMs and explain. (10)

(ii) Explain address translation method in virtual memory. (6)

Or

(b) (i) Explain the various mapping techniques associated with cache memories. (10)

(ii) Write short note on magnetic hard disks. (6)

15. (a) Explain the following :

(i) Interrupts (10)

(ii) Buses. (6)

Or

(b) (i) Explain interface circuits. (8)

(ii) Discuss about PCI buses. (8)

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