Basic DAC Techniques

The schematic of a DAC is shown in fig. The input is an n-bit binary word \( D \) and is combined with a reference voltage \( V_R \) to give an analog output signal.

The \( 0/1 \) of a DAC can be either a voltage or current. For a voltage \( 0/1 \) DAC, the \( D/\text{V} \) converter mathematically described as

\[
V_0 = kV_{fs} \left( d_n 2^{-n} + d_{n-1} 2^{-n+1} + \cdots + d_1 2^{-1} \right)
\]

\( V_0 \) - output voltage
V_{fs} - full scale op. voltage
k - Scaling factor usually adjusted to unity
\( d_1 \) - MSB with a weight of \( V_{fs}/2^1 \)
\( d_n \) - LSB with a weight of \( V_{fs}/2^n \)

Weighted resistor DAC
R-AR ladder
Inverted R-AR ladder.

Weighted Resistor DAC.

One of the simplest circuit shows a summing amplifier with a binary weighted network.

I has \( n \) electronic switches \( d_1, d_2, \ldots, d_n \) controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage \((-V_R)\). And if the input bit is 0, the switch connects the resistor to the ground.

The output current \( I_0 \) for an ideal op-amp can be written as

\[
I_0 = I_1 + I_2 + \cdots + I_n
\]

\[
= \frac{V_R}{2R} d_1 + \frac{V_R}{2^1 R} d_2 + \cdots + \frac{V_R}{2^n R} d_n
\]
The output voltage

\[ V_o = I_0 \frac{R_f}{R} \left( \sum d_i a^{-i} \right) \]

For binary weighted D/A.

i) Although, the op-amp is connected in inverting mode, it can also be connected in non-inverting mode.

ii) The op-amp is working as a current to voltage converter.

iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used.

For example, for TTL compatible switches, the reference voltage should be +5V, and the op will be negative.
One of the disadvantages of binary weighted type DAC is the wide range of resistance values required. It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bit increases, the range of resistance value increases.

For 8-bit DAC, the resistors required are $2^0 R$, $2^1 R$, $2^2 R$, ..., $2^7 R$. The largest resistor is 128 times the smallest one for only 8-bit DAC. The fabrication of such a large resistance in IC is not practical.

Also, the voltage drop across such a large resistor due to the bias current would also affect the accuracy.

![Diagram of totem pole MOSFET switch](image)
A single-pole Mosfet driver in Fig. feeds a resistor connected to the inverting input terminal of Fig. The two complementary gate inputs Q and Q over come from Mosfet S-R flip-flop or a binary cell of a register which holds one bit of digital information to be converted to an analog number. Assume a negative logic logic '1' corresponds to -10v and logic '0' corresponds to zero volt.

If there is '1' in the bit line, S = 1 and R = 0 so that Q = 1 and Q = 0. This drives the transistor Q1-on, thus connecting the resistor R1 to the reference voltage -VR. Whereas the transistor Q2 remains off.

Similarly, a 0 at the bit line connects the resistor R2 to the ground terminal.

Another SPDT switch of Fig. consist of an op-amp. The output of the op-amp feeds a CMOS inverter feeding an op-amp voltage follower which drives Q1 from a very low output resistance. The circuit is using a positive logic with V(1) = VR = +5v and V(0) = 0v.

The complement Q of the bit under consideration is applied at the input.
Thus \( \overline{\alpha} = 0 \) makes transistor \( Q_1 \)-off and \( Q_2 \)-on.

The output of the CMOS inverter is at logic 1 that is, 5V is applied to resistor \( R_1 \) through the voltage follower. And if \( \overline{\alpha} = 1 \) the output of the CMOS inverter is 0V connecting the resistance \( R_1 \) to ground.

\[ V_R(5V) \]

\[ Q_1 \]

\[ Q_2 \]

\[ \overline{\alpha} \]

CMOS Inverter as switch.

Another SPDT switch of Fig. 1 consists of CMOS inverter feeding an op-amp voltage follower which drives \( R_1 \) from a very low output resistance. The circuit is using a positive logic resistance.

With \( V(I) = V_A = +5V \) and \( V(C) = 0V \), the complement \( \overline{\alpha} \) of the bit under consideration is applied at the input. Thus \( \overline{\alpha} = 0 \) makes transistor \( Q_1 \)-off and \( Q_2 \)-on.
The output of the CMOS inverter is at logic 1, if 5 V is applied to resistor $R_1$ through the voltage follower. And if $O = 1$, the output of the CMOS inverter is 0 V connecting the resistance $R_1$ to ground.

R-2R Ladder DAC:

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC, where only two values of resistors are required. It is well suited for integrated chip realization. The typical value of $R$ ranges from 10 kΩ to 100 kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. a, where the switch position $d_1, d_2, d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. b, and finally to Fig. c.

$$\frac{-V_R (2/3 R)}{2R + 2/3 R} = -\frac{V_R}{4}.$$
The output voltage is

\[ V_0 = -\frac{2R}{R} \left( -\frac{V_R}{4} \right) \]

\[ = \frac{V_R}{2} = \frac{V_{FS}}{2}. \]
The switch position corresponding to the binary word 001 in a 3-bit DAC is shown in the diagram.

The output voltage is given by

\[ V_o = \left( \frac{-V_R}{R} \right) \cdot \left( \frac{-V_R}{16} \right) \]

\[ = \frac{V_R}{8} \]
\[ = \frac{V_{fs}}{8} \]

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.
High speed Sample and hold circuit.

Fig. 1 shows a sample and hold circuit for high speed of operation. The Mos transistor M shown is an analog switch capable of switching by logic levels such as that from TTL. It alternately connects and disconnects the capacitor C to the output of op-amp A1.

Diodes D1 and D2 are inverse-parallel connected. They prevent op-amp A1 from getting into saturation when the transistor M is off. This makes the operation of the circuit faster.

Hence the gain of op-amp A1 will be

\[ V_o(t) = V_i(t) - 0.7V \quad \text{when} \quad V_i(t) < V_{OL} \]
and \( V_{o(1)} = V_{i(1)} + 0.7v \) when \( V_{i(1)} > V_{o(1)} \).

When transistor \( M \) is ON, the op-amps \( A_1 \) and \( A_2 \) act as voltage followers. The transistor \( M \) is alternately switched on and off by the control voltage \( V_s \) at its gate terminal. Note that the voltage \( V_s \) is to be higher than the threshold voltage of the FET. When the transistor is OFF for a short interval of time, the capacitor \( C \) quickly charges or discharges to the value of the analog signal at that instant. In other words, when input \( V_i \) is larger than capacitor voltage \( V_c \) and the transistor \( M \) is OFF, it rapidly charges to the level of \( V_i \) the instant \( M \) switches ON.

Similarly if \( V_c \) is initially greater than \( V_i \), then \( C \) rapidly discharges to the level of \( V_i \) when \( M \) becomes ON.

When \( M \) is OFF, only the input bias current of op-amp \( A_2 \) and gate-source reverse leakage current of FET are effective in discharging the capacitor. Hence, the sampled voltage is held constant by \( C \) until the next sampling instant or acquisition time.
During the sampling time \( t_1 \), \( C_1 \) is charged through the FET channel resistance \( R_{DS(on)} \) and the charging time \( t_1 = 5 \, R_{DS(on)} \, C_1 \). When the capacitor charges to 0.993 of input voltage, during the holding time \( t_2 \), the capacitor partially discharges.

Successive Approximation Converter:

The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just \( n \)-clock periods. An eight-bit converter would require eight clock pulses to obtain a digital output.

Fig. 1 shows an eight-bit converter.

The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error. The SAR operates as follows. With the arrival of the START Command, the SAR sets the MSB \( d_7 = 1 \) with all other bits to zero so that the trial code is 10000000.

The output \( V_I \) of the DAC is now compared with the analog input \( V_a \). If \( V_a \) is greater than the
DAC output $V_d$ then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '0' and further tested.

Functional diagram of the successive approximation ADC.

However, if $V_a$ is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested. Whenever the DAC output crosses $V_a$, the comparator changes state and this can be taken as end of conversion (EOC) command.
<table>
<thead>
<tr>
<th>Correct digital representation</th>
<th>SAR Output Vd at S/H</th>
<th>Comparator Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>11010100</td>
<td>10000000</td>
<td>1 (initial output)</td>
</tr>
<tr>
<td></td>
<td>11000000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11100000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11010000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11011000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11010100</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11010110</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11010101</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11010100</td>
<td></td>
</tr>
</tbody>
</table>

**Diagram:***

- **Digital Output**: 12x
- **Actual Analog 8x Vx**: Vx
- **Time**

The diagram illustrates the conversion process from Digital Output to the actual Analog Voltage, showing the relationship between time and voltage levels.
Problem in filter:

Design a fourth-order Butterworth low-pass filter
having upper cut-off frequency 1 kHz.

The upper cut-off frequency $f_h = 1 \text{kHz}$

\[ f_h = \frac{1}{2\pi RC} \]

Let $C = 0.1 \mu F$

\[ R = \frac{1}{2\pi f_h C} \]

\[ = \frac{1}{2\pi \times 1 \times 10^3 \times 0.1 \times 10^{-6}} \]

\[ = \frac{10^3}{2\pi \times 0.1} \]

\[ = 16.06 \Omega \]

From table, for $n = 4$ we get two damping factors
namely $\alpha_1 = 0.765$ and $\alpha_2 = 1.848$. Then the pass band gain of two quadratic factors are

\[ A_{01} = 3 - \alpha_1 \]

\[ = 3 - 0.765 = 2.235 \]

\[ A_{02} = 3 - \alpha_2 \]

\[ = 3 - 1.848 \]

\[ = 1.152 \]

The transfer function of fourth-order low-pass Butterworth filter is

\[ \frac{2.235}{s^4 + 0.765s^3 + 1} \]

\[ \times \frac{1.152}{s^2 + 1.848s + 1} \]
Now,

\[
A_{01} = \frac{1 + R_{f1}}{R_{i1}} = 2.235
\]

Let \( R_{f1} = 12.35\, \text{k}\Omega \) and \( R_{i1} = 10\, \text{k}\Omega \), then we get \( A_{01} = 2.235 \)

Similarly,

\[
A_{02} = \frac{1 + R_{f2}}{R_{i2}} = 1.152
\]

Let \( R_{f2} = 15.2\, \text{k}\Omega \) and \( R_{i2} = 100\, \text{k}\Omega \), which gives \( A_{02} = 1.152 \)

Realization of 4th order Butterworth low-pass filter.
Design a wide-band pass filter having \( f_c = 4 \text{kHz} \) and pass band gain of 4. Find the value of \( Q \) of the filter.

Dual-slope ADC.

The fig shows the functional diagram of the dual slope or dual-ramp converter.

The analog part of the dlt consists of a high input impedance buffer \( A_1 \), precision integrator \( A_2 \), and a voltage comparator.

The converter first integrates the analog input signal \( V_a \) for fixed duration of \( 2^N \) clock periods shown in fig.

Then it integrates an internal reference voltage \( V_r \) of opposite polarity until the integrator output is zero.

![Functional diagram of dual slope ADC](image_url)
The Number N of clock cycles required to return the integrator to zero is proportional to the value of Va averaged over the integration period. Hence, N represents the desired output code.

Before the START command arrives, the switch SW1 is connected to ground and SW2 is closed.

Any offset voltage present in the A1, A2, comparator loop after integration, appears across the capacitor C2 till the threshold of the comparator is achieved.

The capacitor C2 thus provides automatic compensation for the input offset voltages of all the three amplifiers.

At the arrival of the START command at t=t1, the control logic opens SW2 and connects SW1 to Va and enables the counter starting from zero.
The Ch is an n-stage ripple counter
and therefore the counter resets to zero after
counting $2^n$ pulses.

The counter resets itself to zero at the
end of the interval $T_1$ and the switch $SW_i$ is
connected to the reference voltage (-VR). The Op voltage
$V_o$ will now have a positive slope.

As long as $V_o$ is negative, the Op of the
comparator is positive, and the control logic allows the
clock pulse to be counted.

However, when $V_o$ becomes just zero
at time $t_1 = t_2$, the control logic allows the clock
pulse to be counted.

However, when $V_o$ becomes just zero at
time $t_2 = t_3$, the control logic issues (EOC) command.

And no further clock pulses enter the counter.

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{Clock rate}}$$

And

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{Clock rate}}$$

For an integrator

$$\Delta V_o = \left(-\frac{1}{RC}\right) \cdot V(DT)$$
The voltage $V_0$ will be equal to $V_1$ at the instant $t_2$ and can be written as

$$V_1 = \left(-\frac{1}{RC}\right) Va(t_2-t_1)$$

The voltage $V_1$ is also given by

$$V_1 = \left(-\frac{1}{RC}\right) (-V_R) (t_2-t_3)$$

So,

$$Va(t_2-t_1) = V_R (t_3-t_2)$$

putting the values of $(t_2-t_1) = 2^n$

and $(t_3-t_2) = N$, we get

$$Va(2^n) = (V_R) N$$

$$Va = (V_R) \left(\frac{N}{2^n}\right)$$

Advantage

The dual-slope ADC integrates the input signal for a fixed time, hence it provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time $T_1$.

The main disadvantage of the dual-slope ADC is its long conversion time.

Single Slope Type A/D Converter:

These converter techniques are based on comparing the unknown analog input voltage with a reference voltage that begins at $0V$.
A/D Converter using Voltage to Time Conversion

In an A/D converter using V/f converter, the cycles of a variable-frequency source are counted for a fixed period.

Alternatively, it is possible to make an A/D converter by counting cycles of fixed-frequency source for a variable period; for this the analog Vtg is required to be converted to a proportional time period.

Schematic Clt of an A/D converter using voltage to time converter.
A negative reference, $V_A - V_{R}$, is applied to an integrator, whose output is connected to the inverting input terminal of the comparator. The analog voltage is applied at the non-inverting input terminal of the comparator.

The output of the comparator $V_c$ is at logic level 1 as long as the output of the integrator $V_o$ is less than $V_A$. When $V_o$ crosses $V_A$ at $t = T$, $V_c$ goes low. The AND gate is enabled when $V_{EN}$ is low and switch $S$ remains open. When $V_{EN}$ goes high, the switch $S$ is closed, thereby discharging the capacitor. Also, the AND gate is disabled when AND gate is enabled, the clock pulses will reach the counter.

The output of the counter is the digital output corresponding to $V_A$.

The time $T$ is given by

$$T = \frac{V_A}{V_{R}}$$
A/D Converter using Voltage to Time Conversion

In an A/D converter using V/f converter, the cycles of a variable-freq. source are counted for a fixed period.

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Schematic cut of an A/D converter using voltage to time converter.
Which shows that $T$ is proportional to $V_a$.

The counter reading $n$ at $t = T$

then $n = f_c \cdot T$

$= \frac{f_c \cdot V_a}{V_k}$

$f_c$ - Clock Frequency

The count $n$ is proportional to $V_a$.

Specifications for D/A converters:

1. Resolution
2. Linearity
3. Accuracy
4. Settling time
5. Temperature Sensitivity
6. Monotonicity
7. Conversion time
8. Stability

Resolution:

The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter.

Resolution (in volts)

$$= \frac{V_{fs}}{2^7 - 1} = 1.58 \text{ increment}$$

Oversampling A/D converter

V/I Mode & Current Mode R-2R Laddertypes

Single Slope ADC